

Amendments to the Claims

1. (CURRENTLY AMENDED) A data processing system comprising
- a processor (P) and a memory hierarchy, wherein the highest ranked
level in the hierarchy is a cache coupled to the processor, wherein
- a higher ranked cache (C1) in the memory hierarchy has a cache
controller (CC1) operating according to a write allocate scheme,
- a lower ranked cache (C2) is coupled to the higher ranked cache (C1)
and has a cache controller (CC2),
wherein the size of the higher ranked cache is smaller than the size of
the lower ranked cache,
wherein both caches (C1, C2) administrate auxiliary information (V1,
V2) indicating whether data (D1, D2) present therein is valid,
characterized in that,
the linesize of the lower ranked cache (C2) is an integer multiple of the linesize of the
higher ranked cache (C1), wherein the auxiliary information (V1) in the higher ranked
cache (C1) concerns data elements (D1) at a finer granularity than that in the lower
ranked cache (C2) and wherein the higher ranked cache (C1) is arranged for
transmitting a writemask (WM) to the lower ranked cache (C2) in conjunction with a
line of data (DL) for indicating which data in the lower ranked cache (C2) is to be
overwritten at the finer granularity, the cache controller (CC2) of the lower ranked
cache being arranged for fetching a cache line from the next lower ranked level (M) in
the memory hierarchy if that line is not cached yet and the writemask (WM) indicates
that the data in the line provided by the higher ranked cache (C1) is only partially
valid, and wherein fetching a line from said next lower ranked level (M) is suppressed
if the writemask (WM) indicates that the line provided by the higher ranked cache
(C1) is valid in accordance with the coarser granularity of the auxiliary information
(V2) in the lower ranked cache (C2), in which case, the controller (CC2) of the lower
ranked cache allocates the cache line in the lower ranked cache (C2) without fetching
it.

2. (CURRENTLY AMENDED) Data processing system according to claim
1, comprising one or more further processors (P, P', P''), and wherein the memory

hierarchy comprises a memory (M) having a rank which is lower than the rank of said lower ranked cache ($C2$) and which is shared with said other processors.

3. (CURRENTLY AMENDED) Data processing system according to ~~claim 1~~ or ~~2~~claim 1, wherein the cache lines of the lower ranked cache ($C1$) and the higher ranked cache have the same number of data elements.

4. (CURRENTLY AMENDED) Data processing system according to ~~one of the previous claims~~claim 1, wherein the higher ranked cache ($C1$) is a write only cache.

5. (CURRENTLY AMENDED) Data processing system according to ~~one of the previous claims~~claim 1, wherein the higher ranked cache ($C1$) has exactly one cache line.

6. (CURRENTLY AMENDED) Method for operating a data processing system comprising a processor (P) and a memory hierarchy, wherein the highest ranked level in the hierarchy is a cache coupled to the processor, wherein

- a higher ranked cache ($C1$) in the memory hierarchy has a cache controller ($CC1$) operating according to a write allocate scheme,
- a lower ranked cache ($C2$) is coupled to the higher ranked cache ($C1$) and has a cache controller ($CC2$),
wherein the size of the higher ranked cache ($C1$) is smaller than the size of the lower ranked cache ($C2$),
wherein both caches ($C1, C2$) administrate auxiliary information ($V1, V2$), indicating whether data present ($D1, D2$) therein is valid, characterized in that, the linesize of the lower ranked cache ($C2$) is an integer multiple of the linesize of the higher ranked cache ($C1$), wherein the auxiliary information in the higher ranked cache ($C1$) concerns data elements at a finer granularity than that in the lower ranked cache ($C2$), according to which method

- the higher ranked cache (C1) transmits a writemask (WM) to the lower ranked cache (C2) in conjunction with a line of data (DL) for indicating which data in the lower ranked cache (C2) is to be overwritten at the finer granularity,
- the cache controller (CC2) of the lower ranked cache (C2) fetches a cache line from the next lower ranked level (M) in the memory hierarchy if that line is not cached yet and the writemask (WM) indicates that the data in the line provided by the higher ranked cache (C1) is only partially valid, and
- wherein fetching a line from said next lower ranked level (M) is suppressed if the writemask (WM) indicates that the line provided by the higher ranked cache (C1) is valid in accordance with the coarser granularity of the auxiliary information (V2) in the lower ranked cache (C2), in which case, the cache controller (CC2) of the lower ranked cache (C2) allocates the cache line in the lower ranked cache (C2) without fetching it.